EE 434

Lecture 39

- timing of logic circuits
- Power dissipation

Reminder: Exam Friday

Review from last time

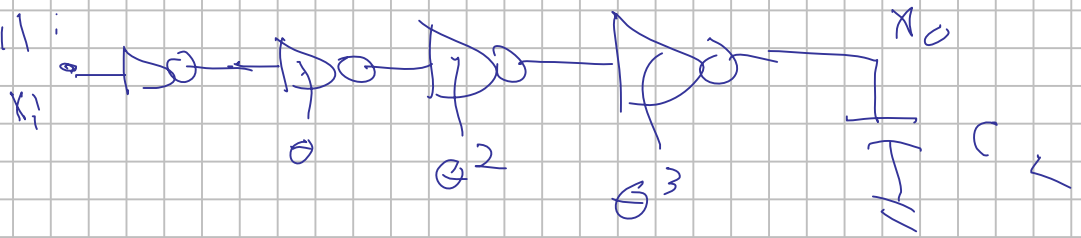
- Elmore Delay
  - way to approximate delay through higher-order RC networks (ladder-type networks)
- Logical Effort
- Ring Oscillators

n is odd
n is usually prime

- widely used for square-wave generation when accuracy of clock is not critical
- crystal used when accuracy is required
- VCO (change f with an electrical variable!)

Pad drivers (drivers)

Recall:



- $\theta_{opt} = e$

typ $\theta = 2, 2.5, 3$

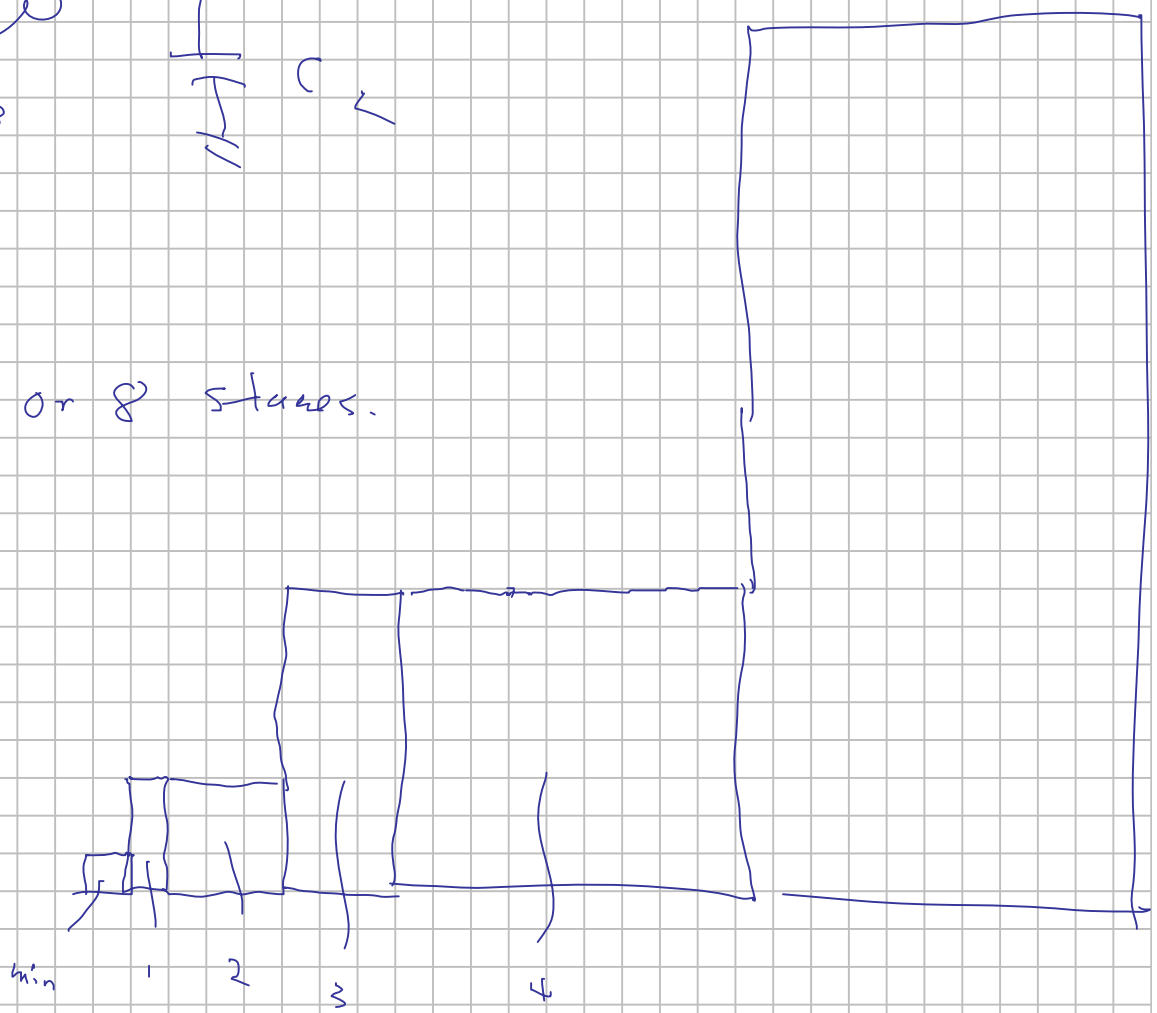
- often to go off chip, need 7 or 8 stages.

Assume $n = 8$, $\theta = 3$

$W_{n8} = 3^8 W_{min} = (6561) W_{min}$

$W_{np} = 3(3^8) W_{min} \approx 19000\ W_{min}$

6500 + 19000



- The large area is almost always justified
  ⇒ if speed problem can be overcom with this type of driver
- Clever layout techniques often used to lay out these drivers
- p-cells specifically available for generating K-stage driver
- Drivers are generally available as part of a pad frame
- Usually do not need to create the pad driver yourself

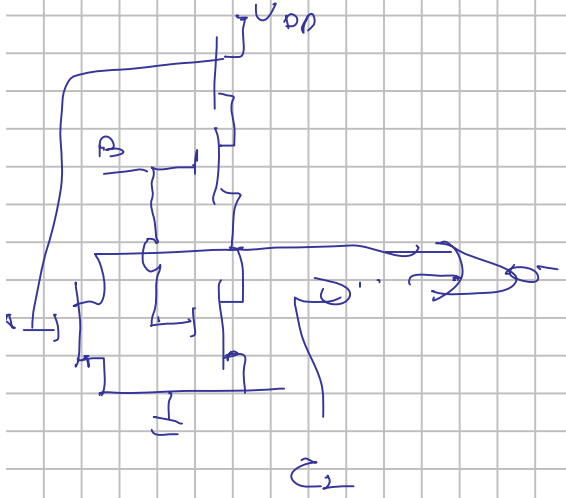
How much faster are equal rise/fall sized circuits than minimum sized circuits?

t_{PROP} = t_{PROP}

Symmetry

$t_{LH} > t_{HL}$

Consider 2-input NOR gate



$R_{PD} = R_{PDR}$

$R_{PU} = 6 R_{PDR}$

$C_L = 2 C_{ox} W_{min} L_{min} = \frac{C_{REF}}{2}$

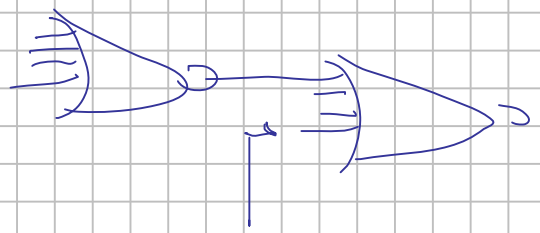
$t_{PROP} = t_{HL} + t_{LH} = \frac{C_{REF}}{2}(6 R_{PDR} + R_{PDR}) = \frac{7}{2} C_{REF} R_{PDR}$

$C_L = C_{ox} W_1 L_1 + 6 C_{ox} W_1 L_1 = 7 C_{ox} W_1 L_1$

for equal rise/fall Hes $\therefore t_{PROP} = 2 R_{PDR} (7 C_{ox} W_1 L_1) = 14 R_{PD} C_{ox} W_1 L_1 = 14 R_{PD} \frac{C_{REF}}{4} = \frac{7}{2} R_{PD} C_{REF}$

Consider n- input NOR gate

1) Equal Rise & Fall Times



$$C_{in} = \frac{3n+1}{4} C_{REF}$$

$$t_{PROP} = 2 R_{pdR} \left(\frac{3n+1}{4} C_{REF} \right) = \frac{3n+1}{2} R_{pdR} C_{REF}$$

2) Minimum Rise & Fall time

$$C_{in} = \frac{C_{REF}}{2}$$

$$R_{pd} = R_{pdR}$$

$$R_{dn} = 3n R_{pdR}$$

$$\therefore t_{PROP} = \frac{C_{REF}}{2} (R_{pdR} + 3n R_{pdR}) = \frac{3n+1}{2} R_{pdR} C_{REF}$$

define γ to be ratio of C_{in}

$$\gamma = \frac{C_{in} \text{ - equal rise/fall}}{C_{in} \text{ min sized}}$$

$$= \frac{\frac{3n+1}{4} C_{REF}}{\frac{C_{REF}}{2}}$$

$$\gamma = \frac{3n+1}{2}$$

Consider n - input NAND gate for both equal rise/fall time and minimum sized transistors

$t_{PHL} = \left(\frac{3+n}{2}\right) t_{REF}$

$\gamma_{NAND} = \frac{C_{in,\,Equal\ Rise/Fall}}{C_{in}\ (Min\ Sized)} = \frac{(3+n)\frac{C_{REF}}{4}}{\frac{C_{REF}}{2}} = \frac{3+n}{2}$

$\frac{3n+1}{2}$

$\frac{3+n}{2}$

For n large, $\gamma_{NAND} << \gamma_{NOR}$

Power Dissipation

4 types

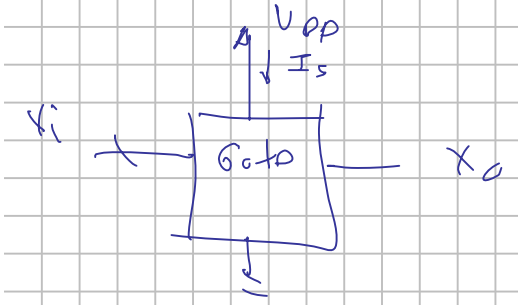
1) Static
2) Dynamic
3) "Pipe"
4) Leakage

$P_{TOTAL} = P_{STATIC} + P_{DYNAMIC} + P_{PIPE} + P_{Leakage}$

often $P_{PIPE} << P_{TOT}$ and can be neglected

$P_{LEAKAGE}$ { $<< P_{Total}$ for .25μ and larger
$\leq P_{TOT}$ for 60 nm and smaller

Static



when X_o is low, I_{SL} flows from V_{DD}

X_o is high, I_{SH} flows from V_{DD}

$$P_{STATIC} = \frac{P_{STATIC\,H} + P_{STATIC\,L}}{2}$$

$$P_{STATIC} = \frac{V_{DD}(I_{SH} + I_{SL})}{2}$$

want to make $I_{SH} + I_{SL}$ as small as possible

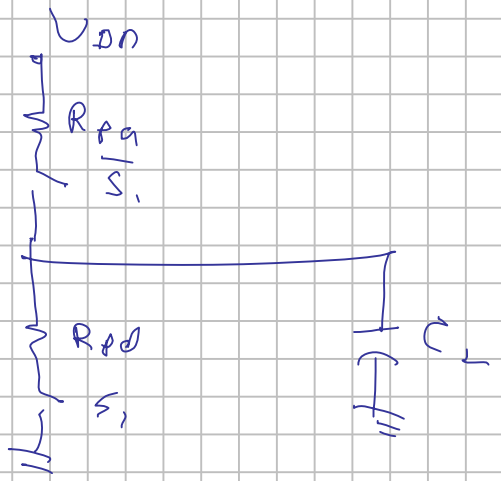
- for static CMOS Logic, $P_{STATIC} \approx 0$
- for NMOS Logic, P_{STATIC} was high & this was the major reason NMOS logic has been replaced with CMOS

Dynamic Power Dissipation

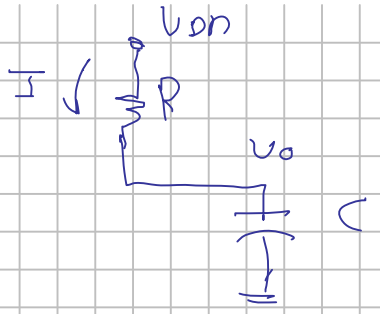
- Power dissipated due to charging & discharging capacitors during logic transitions

- Capacitors do not dissipate any power ☺
- Circuits that charge & discharge capacitors can dissipate considerable energy ☹

Consider



- while charging, current flows through R_{pu} & power is dissipated
- Some energy will be stored
- while discharging C_L, current flows through R_{pd} & power is dissipated



$$E = \int_0^\infty V_{DD}\, I(t)\, dt$$

$$I = C\frac{dv_o}{dt}$$

$$\therefore E = V_{DD}\int_0^\infty C\frac{dv_o}{dt}\,dt$$

$$= C V_{DD}\int_0^\infty \frac{dv_o}{dt}\,dt = C V_{DD}\int_{v_o=0}^{V_{DD}} 1\, dv_o$$

$$E = C V_{DD}^2$$

$$E_{CAP} = \frac{1}{2} C V_{DD}^2 = \frac{E}{2}$$

$\therefore \frac{E}{2}$ is dissipated in R

$\frac{E}{2}$ is temp. stored on C but dissipated during Δt_2

$$\therefore E_{TOTAL} = C V_{DD}^2$$

$$P_{dynamic\ clock} = \frac{E}{T} = f_{CL} C V_{DD}^2$$

$$P_{dynamic\ clock} = f_{CL} C V_{DD}^2$$

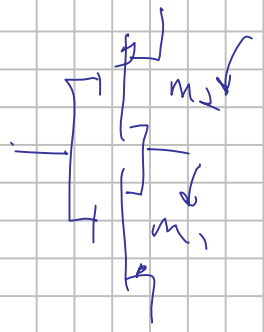
For such logic, $P_{dynamic} = \frac{1}{2} P_{dynamic\ clock} = \frac{1}{2} f_{CL} C V_{DD}^2$

If duty cycle is Θ

$$P_{dynamic} = \Theta f_{CL} C V_{DD}^2$$

major source of power dissipation in circuits with feature sizes above .25μ

P_{PIPE}



- During transition, M_1 & M_2 may both be partially conducting current that "shoots through" M_1 & M_2 is termed pipe current

$$P_{PIPE} = \int V_{DD} I_{PIPE} \, dt$$

- usually I_{PIPE} exists only for a very short time, P_{PIPE} often small
- Fast clock transitions cause small P_{PIPE}